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Final Project Report

for a

Low Magnetic Field Aerospace Memory

June 8, 1967

Under

Contract: NAS 5-9064

Prepared by

DI/AN Controls, Inc.
944 Dorchester Avenue
Boston, Massachusetts 02125

for

National Aeronautics and Space Administration
Goddard Space Flight Center
Greenbelt, Maryland

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ABSTRACT

This document is the final report on a joint NASA-Di/An program to develop a 512 x 12 random access,low power, low magnetic field, low volume aerospace memory.

The following techniques were achieved in the design and construction of this memory:

1. Use of microminiature components and integrated circuits.
2. Memory organization and circuit design aimed at minimizing the number of components and power consumption.
3. Use of non-magnetic materials for minimal interference with satellite experiments. With the improvement within the last year in hybrid circuit techniques, it is highly recommended that an investigation be initiated to utilize hybrid micrologic in place of the discrete circuits. Using the above techniques combined with hybrid micrologic would be a significant breakthrough for the memory industry.
4. Power-enabling techniques significantly reduced the operating power consumption.
5. Complementary transistor circuit designs were utilized to reduce standby power.
6. An efficient and compact mechanical design was developed.
7. Selection of light-weight materials for structure and encapsulation.
8. Use of small cores (0.030" O.D.) closely spaced (on 0.030" centers).

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SECTION 1

HISTORY OF PROJECT

Below is a brief summary of the work that was accomplished during the following periods.

CONCEPTUAL STUDY - March 30, 1965-June 30, 1965

A study was begun centering on the magnetic properties of the components to be used in the memory. The study has taken three courses:

a. Liaison with other workers in the field of low magnetic disturbance components.
b. Survey of the literature on the topic.
c. Experimental set-up was constructed at DI/AN for magnetic testing of components.

MAGNETIC AND PRELIMINARY CIRCUIT CONFIGURATION - June 30, 1965-October 5, 1965

An investigation of the magnetic properties of tape wound cores and transistors compared with hybrid circuit techniques revealed that a substantial decrease in the magnetic field could be obtained if hybrid circuits were used in the system. Various hybrid circuit manufacturers were contacted.

The results of the circuit design including addressing and logic circuitry, interface circuitry, and memory stack are stated. It was concluded that maximum reliability could be obtained if hermetic sealing techniques are utilized.

COMPUTER ANALYSIS AND CIRCUIT SELECTION - October 5, 1965-January 8, 1966

Worst case analysis, both theoretical and machine computer design of the basic memory circuits was completed. The entire system was realized with essentially non-magnetic materials.

Magnetic testing of circuit components and hardware was initiated both at DI/AN and NASA. After consultations with personnel at NASA-Langley and NASA-Goddard, a decision was made to use hybrid micrologic of a type similar to that produced by vendors,National Semiconductor and Sprague Electronics Corporation. These techniques would have guaranteed that the design goals of low magnetic field, low power, low weight and volume could be met.

CONFIGURATION ESTABLISHMENT AND CIRCUIT PURCHASE - January 8, 1966-March 31, 1966

Circuit design was completed, memory configuration was decided upon and significant advances were made in the definition of a packaging technique. In addition, calculations based on the use of hybrid circuits to be contained in the memory indicated that the magnetic field requirements which were considered as design goals could be met.

Negotiations were begun with National Semiconductor.

SENSE AMPLIFIER SELECTION AND CONTINGENCY PROGRAM - March 31, 1966-June 30, 1966

A detailed analysis of the Motorola sense amplifier was accomplished. In addition, memory system breadboard data was gathered and analyzed.

The procurement of hybrid circuits was delayed because National Semiconductor was unable to meet its commitment to supply the circuits.

A contingency program using discrete micro-miniature components was initiated in anticipation of the possibility that the hybrid vendors would be unable to meet the stringent requirements of the program.

DESIGN RE-DIRECTION AND PRODUCTION ESTIMATES - June 30, 1966-October 15, 1966

After negotiations with both Amperex Electronic Corporation and Fairchild Semiconductor Corporation, it was decided to complete the memory on schedule using the discrete components, selected in the contingency program in modular construction. The final selection of parts, including module sizes and preliminary printed circuit layouts were accomplished. Revised estimates of weight and volume were calculated.

DRAFTING, ASSEMBLY AND TESTING - October 15, 1966-January 15, 1967

System and subsystem assemblies were being completed with complete system testing to begin January 30, 1967.

FINAL TEST AND DELIVERY - January 15, 1967-April 7, 1967

Final system testing completed and shipped.

SECTION 2

MEMORY DESCRIPTION

2.1 GENERAL DESCRIPTION

The memory described in this manual is a random-access, coincident-current memory system that has a capacity of 512, twelve-bit words. The memory was developed to yield a very low operating power requirement and to produce a very low external magnetic field. High reliability and high component density were achieved by the utilization of microminiature components in encapsulated modules. Wide temperature environments are made possible by the use of lithium-ferrite cores in the memory planes.

Power enabling techniques were used to hold operating power to a very low level for a memory of this size. These, combined with complementary circuit designs produced an exceptionally low standby power requirement.

All components in the memory were selected and packaged for minimum magnetic disturbance.

2.2 FUNCTIONAL DESCRIPTION

2.2.1 ACCESS MODE

The memory is designed for random addressing on nine, single-rail lines entering in parallel. The address data must remain steady for the entire memory cycle time as no internal address register is incorporated in this memory.

2.2.2 DATA INPUT/OUTPUT

The data to be stored in the memory is supplied on twelve, single-rail lines and must be entered in parallel. The data lines must be held steady for the complete memory cycle as this system does not employ an input (or output) data register.

The output data is supplied on twelve single-rail lines in parallel. The data out is the complement of the stored (input) data.

2.2.3 OPERATION MODES

This memory system is a full-cycle, two-mode type which permits either a standard Clear/Write or a Read/Restore mode of operation.

Clear/Write: In this mode, stored data at a given address(es) is erased and new data is inserted in its place.

Read/Restore: The stored data is retrieved in this mode, and placed on the output data lines for use by external equipment. The data is re-loaded into its original address in the memory during the Restore phase of the memory cycle.

2.3 PHYSICAL DESCRIPTION

The memory is housed in a compact aero-space type housing. Refer to the Outline and Mounting drawing, C-2204-4010, located in the drawing section of this manual for the physical dimensions.

2.4 GENERAL SPECIFICATIONS

2.4.1 MEMORY OPERATING SPECIFICATIONS

Operating Frequency (max.):	45 K.C.
Memory Cycle Time:	22 usec.
Access Time:	8 usec.
Storage Capacity:	512 x 12

Interface Logic Levels:	Logical ZERO - Gnd. (sat. NPN transistor) Logical ONE - +3.3 Volts ±10%

Note: The interface circuits have been designed to interface with Texas Instruments, Series 51, Solid State circuits

Access Mode:	Random
Operating Modes:	Clear/Write and Read/Restore

2.4.2 INTERFACE SPECIFICATIONS

Mode Sync. In (2 lines)	Clear/Write Command and Read/Restore Command: A positive pulse from logic "0" to logic "1" on individual lines Width: 4.5 usec max. Rise Time: 1.6 usec max.
Address Data:	Single Rail Logic Levels: Must be valid at sync time and remain valid during complete memory cycle
Input Data:	Single Rail Logic Levels: Must be valid at sync time and remain valid during complete memory cycle
Output Data:	Single Rail Logic Levels Complement of Input Data: Data is present for a maximum of 4.5 usec. with a rise time of 1.6 usec. max. Access time is approximately 8 usec. from sync time but may be shortened to 4.5 usec. with reduced margins.

2.4.3 ENVIRONMENTAL SPECIFICATIONS

Operating Temperature Range:	$-20^{o}C$ to $+85^{o}C$
Storage Temperature Range:	$-55^{o}C$ to $+125^{o}C$

2.4.4 POWER REQUIREMENTS

Power Supplies Required:	+6 VDC ±2%
	-6 VDC ±2%
	+3.3 VDC ±2%
Power Required Operating:	1.15 Watts
Power Required Standby:	3.49 MW.

2.4.5 PHYSICAL SPECIFICATIONS

Volume:	62 cubic inches
Weight:	2 lb., 10 oz.

2.4.6 SHOCK AND VIBRATION SPECIFICATIONS

Shock:	40g., 8 msec.
Vibration:	2g. @16-42 cps
	0.022 inch double amplitude
	at 42-95 cps
	10g. @95-2000 cps

2.4.7 HUMIDITY

To 100% R.H. without condensation

SECTION 3

FINAL TESTING AND DATA

3.1 INTRODUCTION

This sectioncontains the operation and tests of the random-access memory developed under NASA contract NAS 5-9064. This unit is a magnetic-core memory capable of storing a 12 bit word in any of 512 address locations and later reading this or any other word non-destructively.

3.1.1 REFERENCE DRAWINGS

The following list of drawings is required to test the memory.

a. Logic diagram D2204-4002.

b. Di/An random-access memory tester Model E-1599, C2204-4010.

3.1.2 TEST EQUIPMENT

Power Supplies

No.	Voltage	Regulation *	Current Capability
1	+6v	± 1%	600 ma
2	-6v	± 1%	600 ma
3	+3.3v	± 1%	300 ma

* Includes variation of voltage due to line, load and drift.

a. OSCILLOSCOPE

Tektronix No. 547 with type ca dual trace pre-amp and 2-type P6006 x 10 passive probes or equivalent instrument.

b. MEMORY FUNCTIONAL TESTER

Di/An random-access memory tester Model E-1599.

c. OVEN

Associated Testing Laboratories, Inc. or similar.

d. PRECISION DC VOLTMETER

Weston Model 911 or equivalent.

e. Simpson Model 260 Volt-ohm - milliameter or equivalent.

3.2 FUNCTIONAL OPERATION OF MEMORY TESTER AND MEMORY

This section outlines the capabilities of the memory self tester as used to test the memory. The controls and indicators on the tester are explained in detail.

3.2.1 CLOCK

This pulse is used to advance the address counter.

3.2.2 "MODE" SWITCH

When this switch is in the "Clear/Write" position it applies a positive going pulse from ground to the Clear/Write input of the memory, causing the memory to clear (destroy) old data and write new data. Placing the "mode" switch in the "Read/Restore" position applies a positive going pulse to the "Read/Restore" input of the memory and data previously stored in the memory is read out and restored.

3.2.3 DATA SWITCH

Four types of data input may be selected, all "one", all "zero", worst-word and worst-word complement.

3.2.4 "ERROR" SWITCH

The memory tester compares data entered in a particular address with data read from that address for error, and lights an error lamp when an error occurs. The tester takes no further action if the error switch is in the F/R ("Free Run") position. However, if the error switch is in the "Stop on Error" position, the detected error will close the clock gate which drives the address counter. The address counter is stopped at the address containing the error. This address may be read from the front panel as a binary coded number. Although the address counter is gated off, memory initiate pulses are still applied to the memory. Memory output data may be read from the front panel.

3.3 TESTING

All data shall be recorded on a reproducible check list which shall be filed by Di/An Quality Assurance Section.

3.3.1 PREFUNCTIONAL TESTING

3.3.1.1 EXAMINATION

Each unit shall be visually examined to determine that the unit meets the Di/An quality control requirements of workmanship identification, marking, finish and cleanliness.

3.3.1.2 WEIGHT

The weight of the unit shall be measured to the nearest ounce.

3.3.1.3 VOLUME

Each unit shall be inspected for dimensional conformance as per Di/An Drawing C2204-4010.

3.3.2 **FUNCTIONAL TESTING**

3.3.2.1 **TESTS AT 25°C AMBIENT TEMPERATURE.**

All power supplies set within ± 1% of their nominal voltages, and the tester is operated in the Stop on Error mode. The memory mode used in these tests is a Clear/Write operation at every address followed by a continuous Read/Restore operation alone at every address. Table 3-1 contains a list of tests performed at 25°C, test conditions, tester switch settings, data to be recoded, etc. Record data on check list which accompanies this test procedure. All input "One" levels to the memory shall be 3.3v ± 10% through 5k ± 10%.

a. D.C. Power Consumption - Standby Condition

No initiate pulses are to be applied in this test. Use Simpson Model 260 milliameter and measure the current delivered to the memory by each power supply.

b. D.C. Power Consumption - Operating Condition

Set mode switch to alternate "Clear/Write" "Read/Restore" and adjust frequency for 65 microsecond spacing between memory initiate pulses. Set memory tester "Data" switch to all "Zeros". Use Simpson model 260 milliameter to measure current delivered.

c. Output Data Bits (12)

Logic levels timing all "ONES" are written into the memory and then read out. Each of the 12 data output lines is measured with an oscilloscope. Each data output waveform must meet the requirements of figure 1.0 and Table 3-2. The output data is the complement of the input data. A "one" input will produce a "zero" output and a zero input will produce a "one" output.

d. Error Test - All "ONE'S" Input Data

This tests the ability of the memory to Clear/Write and then Read/Restore all "ONE'S" without error. Every address is so tested.

e. Error Test - All "ZERO'S" Input Data

Otherwise the same as 3.3.2.1e.

f. Error Test

Worst Word pattern input data during Clear/Write cycle results in a maximum of Sense noise during Read/Restore cycle. Every address must be read without error.

g. Error Test

Input data is complement of Worst Word pattern; test is otherwise similar to 3.3.2.1f.

h. **Power Turn-Off Test**

Set the "Mode" switch to "Clear/Write". Set the "Data Input" switch to "Worst Word" and load the memory.

Set "Mode switch to "Read/Restore" and set "Error" switch to "Stop On Error." Verify that no errors in memory content or readout exist If no errors occur, perform the following tests for memory message volatility.

Disable the clock and memory initiate pulse. Switch off the three power supplies in the order given in Table 5.0, and short the terminals of each supply as it is switched off Turn on the three power supplies and note that no errors occur as the memory Read/Restores; record this fact on the Check List.

Repeat the power supply turn-off procedure given above for each of the remaining steps (#2 to #6) in Table 5.0. Record the results on the Check List.

3.3.2.2 Tests at -20°C Ambient Temperature

The memory is placed in an oven whose temperature control is adjusted for -20°C A minimum of two hours stabilizing time shall be allowed for the oven to reach -20°C. Initially, all power supplies are set within ± 1% of their nominal voltages. The memory tester will be operated in the "Stop on Error" mode, and the memory cycled in the alternate Clear/Write, Read/Restore mode during each test.

During a given test, each power supply in turn is varied from a high limit voltage through nominal voltage to a low limit voltage while the other three supplies are held at their nominal voltages. Table 3-3 contains a list of these power supply voltage limits, along with tester switch settings and test conditions for each test. Record test data called for in Table 3-3 on the check list which accompanies this test procedure.

3.3.2.3 Tests at +85°C Ambient Temperature

The memory is placed in an oven whose temperature control is adjusted for +85°C. A minimum of two hours stabilizing time shall be allowed for the oven to reach +85°C.

With the exception of ambient temperature, the tests in this section are identical to those of section 3.2.2 and are found in Table 4.0.

INPUT LOADING - SERIES 51, N = 1 EQUIVALENT, -20°C TO +85°C

OUTPUT SIGNAL - SERIES 51, N = 5 LOADS, V_{cc} = 3.3 ±10% VOLTS

SIGNAL REQUIREMENTS

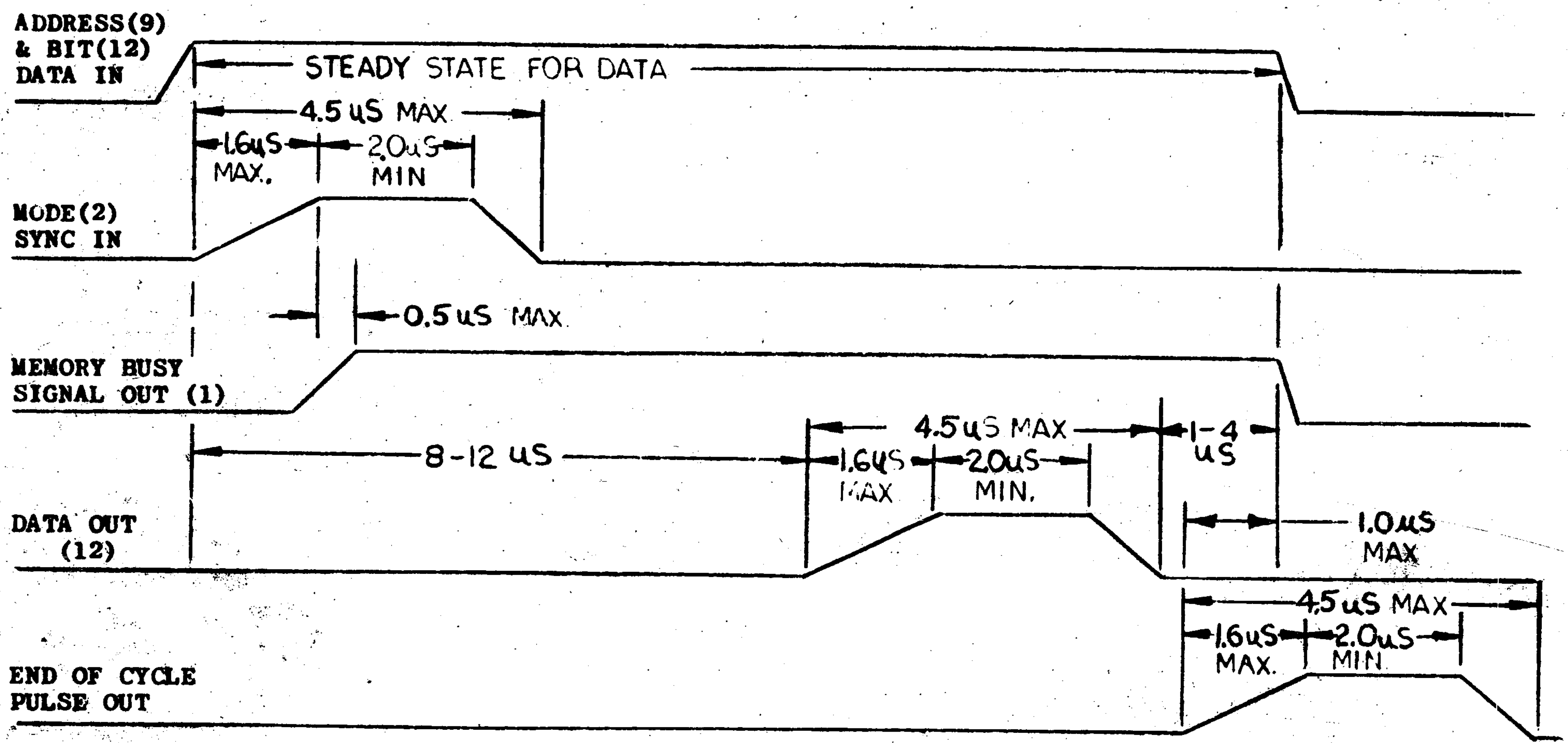

FIGURE 1

INTERFACE SIGNALS

PROJECT E1599

TEST PARAGRAPH AND DESCRIPTION	MEMORY POWER SUPPLY SETTINGS			MEMORY SELF TESTER SWITCH		
	+6V NOM	-6V NOM	+3.3V NOM	CYCLE FREQ. ADJ.	MODE	ERROR DETC.
3.3.2.1a. DC POWER CONSUMPTION - STANDBY CONDITION	+6.00 VOLTS	-6.00 VOLTS	+3.30 VOLTS	15.0 KHZ		N.A.
3.3.2.1b. DC POWER CONSUMPTION - OPERATING CONDITION					ALT C/W R/R	STOP ON ERROR
3.3.2.1c. OUTPUT DATA BITS ($\overline{1}2$) LOGIC LEVELS & TIMING						FREE RUN
3.3.2.1d. ERROR TEST - ALL "ONES" INPUT DATA						STOP ON ERROR
3.3.2.1e. ERROR TEST - ALL "ZEROS" INPUT DATA						
3.3.2.1f. ERROR TEST - "WORST WORD" INPUT DATA						
3.3.2.1g. ERROR TEST - COMPLEMENT OF "WORST WORD" INPUT DATA						
3.3.2.1h. POWER TURN-OFF TEST (DATA RETENTION)						
A. LOAD DATA	+6.00	-6.00.	+3.30		C/W	
B.	TURN-OFF SUPPLIES ACCORDING TO TABLE 5.0 STEP NO.1.					
C.	T [illegible] 3 SUPPLIES ON.				R/R	STOP ON ERROR
D.	REPEAT B AND C ABOVE FOR EACH STEP (#2 TO #6) OF TABLE 5.0 IN ORDER.			15.0 KHZ		

TABLE 3-1 FUNCTIONAL TEST CONDITIONS AT +25°C

TTINGS; TEST CONDITIONS		REQUIRED RESULTS OF TEST.
	DATA WORD	
		MEASURE AND RECORD CURRENT DRAIN ON EACH SUPPLY. RECORD DATA TAKEN ON CHECKLIST.
	ALL "ZEROS"	INITIATE TEST, THEN MEASURE AND RECORD CURRENT DRAIN ON EACH SUPPLY.
	ALL "ONES" ALL "ZEROS"	MEASURE AND RECORD "ONE" LEVEL, "ZERO" LEVEL, AND ACCESS TIME (T1) ON CHECKLIST FOR EACH DATA OUTPUT LINE. SEE FIGURE 1.0 (WAVEFORMS). EACH DATA LINE WAVEFORM SHALL MEET THE LIMITS OF TABLE 3-2.
	ALL "ONES"	"ERROR" LAMP MUST NOT LIGHT DURING TEST.
	ALL "ZEROS"	
	WW	
		"ERROR" LAMP MUST NOT LIGHT DURING TEST.
		A. "WORST WORD" DATA PATTERN LOADED INTO MEMORY.
		B. REMOVE R/R AND CLOCK PULSE BEFORE SWITCHING SUPPLIES OF
		C. REPLACE CLOCK AND R/R PULSE AFTER SWITCHING SUPPLIES ON PUSH "START" PUSHBUTTON. ERROR LAMP MUST NOT LIGHT.
	WW	D. ERROR LAMP MUST NOT LIGHT DURING R/R TEST FOR ANY STEP, #2 TO #6.

TABLE 3-2. SIGNAL OUTPUT LIMITS

OUTPUT CHARACTERISTIC	-20°C LIMIT VALUES	+85°C LIMIT VALUES
DATA OUTPUT "1" LEVEL	+3.0 VOLTS MIN.	+3.0 VOLTS MIN.
DATA OUTPUT "0" LEVEL	+0.3 VOLTS MAX.	+0.3 VOLTS MAX.
DATA OUTPUT ACCESS TIME	30 USEC MAX.	30 USEC MAX.
MEMORY BUSY	+5.0 VOLTS MIN.	+5.0 VOLTS MIN.
END OF CYCLE PULSE	+5.0 VOLTS MIN.	+5.0 VOLTS MIN.

TEST PARAGRAPH AND DESCRIPTION	MEMORY POWER SUPPLY SETTINGS			MEMORY SELF TESTER SWITCH SET		
	+6V NOM	-6V NOM	+3.3V NOM	CYCLE FREQ. ADJ.	MODE	ERROR DETC.
3.3.2.2a. ERROR TEST-ALL "ONES" INPUT DATA	+5.88 TO +6.12	-5.88 TO -6.12	+3.24 TO +3.36	15.0 KHZ	ALT C/W	STOP ON ERROR
3.3.2.2b. ERROR TEST ALL "ZEROS" INPUT DATA	↕	↕	↕	↕	↕	↕
3.3.2.2c. ERROR TEST "WORST WORD" INPUT DATA	↕	↕	↕	↕	↕	↕
3.3.2.2d. ERROR TEST COMPLEMENT OF "WORST WORD" - INPUT DATA	+5.88 TO +6.12	-5.88 TO -6.12	+3.24 TO +3.36	15.0 KHZ	ALT C/W	STOP ON ERROR

TABLE 3-3 FUNCTIONAL TEST CONDITIONS AT -20°C

S; TEST CONDITIONS		REQUIRED RESULTS OF TEST
DATA WORD		
ALL "ONES"		"ERROR" LAMP MUST NOT LIGHT DURING TEST.
ALL "ZEROS"		
WW		
WW		"ERROR" LAMP MUST NOT LIGHT DURING TEST.

ST PARAGRAPH AND SCRIPTION	MEMORY POWER SUPPLY SETTINGS			MEMORY SELF TESTER SWITCH SET		
	+6V NOM	-6V NOM	+3.3V NOM	CYCLE FREQ. ADJ.	MODE	ERROR DETC.
3.2.3a. ERROR TEST- L "ONES" INPUT DATA	+5.88 TO +6.12	-5.88 TO -6.12	+3.24 TO +3.36	15.0 KHZ	ALT C/W	STOP ON ERROR
3.2.3b. ERROR TEST L "ZEROS" INPUT DATA	↕	↕	↕	↕	↕	↕
3.2.3c. ERROR TEST ORST WORD" INPUT TA	↕	↕	↕	↕	↕	↕
3.2.3d. ERROR TEST MPLEMENT OF "WORST ORD" - INPUT DATA	+5.88 TO +6.12	-5.88 TO -6.12	+3.24 TO +3.36	15.0 KHZ	ALT C/W	STOP ON ERROR

TINGS; TEST CONDITIONS

TP-E1599

TABLE 3-4 FUNCTIONAL TEST CONDITIONS AT +85°C

DATA WORD		REQUIR. RESULTS OF TEST
ALL "ONES"		"ERROR" LAMP MUST NOT LIGHT DURING TEST.
ALL "ZEROS"		
WW		
WW		"ERROR" LAMP MUST NOT LIGHT DURING TEST.

TABLE 3-5. POWER SUPPLY TURN-OFF SEQUENCE

ORDER OF TURNING OFF SUPPLIES			
STEP NO.	FIRST	SECOND	THIRD
1	+6	-6	+3.3
2	+6	+3.3	-6
3	-6	+6	+3.3
4	-6	+3.3	+6
5	+3.3	-6	+6
6	+3.3	+6	-6

DI/AN CONTROLS, INC.
944 Dorchester Avenue
Boston, Massachusetts 02125

TEST PROCEDURE

NAS 5-9064

LOW POWER MEMORY

CHECK LIST

Section | Data to Record

3.3.1 PREFUNCTIONAL TESTING

3.3.1.1 Workmanship OK — Identification OK

Marking OK — Finish OK

Cleanliness OK

3.3.1.2 Weight 2 lbs. 10 oz.

3.3.1.3 Dimensional Conformance to Outline Drawing OK

3.3.2 FUNCTIONAL TESTING

3.3.2.1 Tests at +25°C Ambient Temperature

a. DC Power Consumption - Standby

+6 Volt Supply 0.58 M AMP
-6 Volt Supply 11μA. ~~M AMP~~
+3.3 Volt Supply 0.3μA ~~M AMP~~

b. DC Power Consumption - Operating

+6 Volt Supply 76 M AMP
-6 Volt Supply 56 M AMP
+3.3 Volt Supply 110 M AMP

Date 4/7/67 — Serial No. P/N 2209

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c. Output Data Bits

Data Line	"ONE" Level	"ZERO" Level	Access Time, T1
# 1	3.2 Volts	0.1 Volts	8.0 Usec
# 2	3.2 Volts	0.1 Volts	8.0 Usec
# 3	3.2 Volts	0.1 Volts	8.0 Usec
# 4	3.2 Volts	0.1 Volts	8.0 Usec
# 5	3.2 Volts	0.1 Volts	8.0 Usec
# 6	3.2 Volts	0.1 Volts	8.0 Usec
# 7	3.2 Volts	0.1 Volts	8.0 Usec
# 8	3.2 Volts	0.1 Volts	8.0 Usec
# 9	3.2 Volts	0.1 Volts	8.0 Usec
#10	3.2 Volts	0.1 Volts	8.0 Usec
#11	3.2 Volts	0.1 Volts	8.0 Usec
#12	3.2 Volts	0.1 Volts	8.0 Usec

Memory Busy OK

End of Cycle Pulse OK

d. Error Test - All "ONE's" Input Data

Errors NONE

e. Error Test - All "ZERO's" Input Data

Errors NONE

f. Error Test - "Worst Word" Input Data

Errors NONE

g. Error Test - Complement of "Worst Word" Input Data

Errors NONE

h. Power Supply Turn-Off Test

Step No.	Errors
1	None
2	None
3	None
4	None
5	None
6	None

3.3.2.2 Tests at -20^{0}C Ambient Temperature.

Oven stabilized for 2 hrs. 0 min. at -20^{0}C.

Oven final temperature: -20 ^{0}C.

Date 4/7/67

Serial No. P/N 2209

Quality Control Technician M. Mason

Quality Assurance ________

a. **Error Test - All "ONE's" Input Data**

Vary +6 Volt Supply	Errors NONE
" -6 Volt Supply	Errors NONE
" +3.3Volt Supply	Errors NONE

b. Error Test - All "ZERO's" Input Data

Vary +6 Volt Supply	Errors NONE
" -6 Volt Supply	Errors NONE
" +3.3Volt Supply	Errors NONE

c. Error Test - "Worst Word" Pattern Input Data

Vary +6 Volt Supply	Errors NONE
" -6 Volt Supply	Errors NONE
" +3.3Volt Supply	Errors NONE

d. Error Test - "Worst Word Complement" Input Data

Vary +6 Volt Supply	Errors NONE
" -6 Volt Supply	Errors NONE
" +3.3Volt Supply	Errors NONE

3.3.2.3 **Tests at +85°C Ambient Temperature.**

Oven stabilized for 2 hrs. 0 min. at +85°C.

Oven final Temperature 85 °C.

a. Error Test - All "ONE's" Input Data.

Vary +6 Volt Supply	Errors NONE
" -6 Volt Supply	Errors NONE
" +3.3Volt Supply	Errors NONE

b. Error Test - All "ZERO's" Input Data.

Vary +6 Volt Supply	Errors NONE
" -6 Volt Supply	Errors NONE
" +3.3Volt Supply	Errors NONE

Date 9/7/67

Quality Control Technician M. Mason

Serial No. P/N 2204

Quality Assurance ______

c. **Error Test - "Worst Word" Pattern Input Data**

Vary +6 Volt Supply	**Errors** NONE
" -6 Volt Supply	**Errors** NONE
" +3.3Volt Supply	**Errors** NONE

d. **Error Test - "Worst Word Complement" Input Data**

Vary +6 Volt Supply	**Errors** NONE
" -6 Volt Supply	**Errors** NONE
" +3.3Volt Supply	**Errors** NONE

Date 9/7/67

Quality Control Technician M. Mason

Serial No. P/N 2209

Quality Assurance ____________

SECTION 4

TECHNIQUES FOR POWER REDUCTION

4.1 REDUCTION OF DRIVE CURRENT BY USE OF SMALL CORES

The memory core material was chosen to satisfy the requirements for speed and operating temperature range. Once the material was determined, the drive current was determined by the core diameter, the required drive current being directly proportional to the core diameter. Memory cores of 0.030" diameter are available in a material suitable for operation over wide temperature ranges; e.g. Radio Corporation of America 266M1 or Lockheed Electronics Company 30WT02. The RCA 266M1 was used in the memory. The drive current for this core is only 60% of that for a similar material in a 0.050" diameter core, as used in the Apollo Spacecraft computer memory, for example.

Consider the case where all dimensions in the core stack retain the same relative proportions among themselves, and the linear dimensions are allowed to vary. We will now estimate the dependence of power consumption on the linear dimensions. The drive current is proportional to the core diameter. The wire resistance is proportional to the length and inversely proportional to the square of the diameter; hence, is inversely proportional to the linear dimension. I^2R from the two relationships above is proportional to length squared and inversely proportional to length; hence, is proportional to the length dimension. Thus, power consumption is linearly related to the physical dimensions of the system.

4.2 REDUCTION OF REQUIRED SUPPLY VOLTAGE BY REDUCTION OF WINDING RESISTANCE AND INDUCTANCE

The supply voltage for the memory current drivers must be larger than the voltage drop across the core line being driven. This voltage drop is $IR + L\frac{dI}{dt}$. The required supply voltage was reduced by reducing both the core line resistance and inductance. This was done by reducing the length of the core access line. This, in turn, was done by reducing the spacing between cores along a core line. The usual spacing for cores of 0.030" diameter is 0.040", or sometimes 0.030". These close spacings, which can be achieved routinely in production, offer a 40% or greater reduction in both resistance and inductance, as compared with the spacings used with the older 0.050" diameter cores. On an experimental basis, DI/AN has wired a full 4096-bit core plane with 0.030" diameter cores on 0.020" center to center spacing, using an improvement on a proprietary core plane configuration now in routine production with 0.050" diameter cores. Performance figures quoted in this report are on the basis of 0.030" spacing between cores; the experimental core plane mentioned above was duplicated in production, and was incorporated into this memory, with a corresponding improvement in power consumption.

4.3 COMPLEMENTARY TRANSISTOR DESIGN

This memory is built entirely of complementary PNP-NPN logic. Thus, all circuits when not performing their active function, are in the OFF state, drawing only leakage currents. The original design concept forecasts the use of magnetic driving circuits. These circuits inherently consume power only when operating and thus can provide even lower power levels than the complementary logic being used. However, the requirement for low magnetic-signature ruled out the use of large, tape-wound driver cores. By our measurement, and by measurements performed by Mr. Cliff at NASA, the cores contribute a large proportion of the static magnetic field, and the addition of the tape wound drivers would raise the level so high that our other techniques for reducing the field would be a waste of effort. Thus, a certain power sacrifice has been made to achieve a lower magnetic field.

4.4 SENSE AMPLIFIER POWER ENABLING

Standby power measurements of the Motorola SC1219F (formally XC-87) sense amplifier revealed a worst case consumption of 266 milliwatts. By power enabling the sense amplifier this power consumption was practically eliminated.

The standard SC1219F output circuit consists of an NPN transistor with a 6K resistor to the +6 power buss . This circuit will be used to drive a NPN-PNP complementary one-shot with the sense amplifier output from the collector of the output transistor. To power enable the sense amplifier, the 6 volt buss must be disconnected but the one-shots are not power enabled. Therefore, if the sense amplifier output is directly coupled to the one-shot, a sneak path exists from the 6 volt of the data one-shot up through the sense amplifier output collector resistor and down through other resistors connected to the 6 volt buss of the sense amplifier to ground. This path was virtually blocked by coupling the sense amplifier through a high value resistor, in parallel with a capacitor.

4.5 Z-DRIVER VOLTAGE

The Z-driver voltage was at first set at 6 volts. However, a study of the voltage drops in the Z circuit indicated that good operation could be obtained at the 3.3 volt level which is also available and subsequently the Z-driver supply was changed to 3.3 volts. The effect was one of marginal operation with voltage supply variations. This effect was minimized by the selection of temperature compensating resistors and by the selection of transistors for optimum saturation and gain characteristics. A certain amount of long term stability is compromised since component variations will have a larger effect on the Z current. However, the initial selection process can minimize these effects on the Z current. A regulation of ±2% is required on the 3.3 volt power supply.

SECTION 5

ENVIRONMENTAL REQUIREMENTS

Environment:

a) Storage at -55^{o}C to 125^{o}C
b) Operation at -30^{o}C to 85^{o}C
c) Shock: to 40g, 8 msec
d) Vibration: to 2g at 16-42 cps. 0.022 inch double amplitude at 42-95 cps. 10g at 95-2000 cps.
e) Humidity: to 100% R.H. without condensation.

The temperature requirements were met successfully.

Because of the unknown restrictions that were placed on the memory mechanical design, associated with the requirement for low external magnetic field disturbance, the shock and vibration figures were held as design objectives. DI/AN feels, on the basis of the actual test results on its previous aerospace memories, that the vibration and shock specifications can probably be achieved. In any case, best design effort was applied.

SECTION 6

TECHNIQUES FOR SIZE AND WEIGHT REDUCTION

The following techniques were applied to minimize the size and weight of this memory.

6.1 COMPONENTS

Microminiature components and integrated circuits were utilized where possible. The selected components are the Bourns Microresistor, the Microdiode of Microsemiconductor Corp. and Fairchild transistors packaged in their Hermet case. Utilizing the above components packaged in the DI/AN standard pico-bit module (3/8 x 5/8 x .35) a great reduction in size and weight was achieved.

6.2 CORE PLANES

The core plane was built using small cores (0.030" O.D.), closely spaced (on 0.030" centers). This arrangement not only saved space but a power savings also resulted as explained in Section 4, Techniques for Power Reduction.

6.3 MECHANICAL DESIGN

The system layout and mechanical design was accomplished in an efficient and compact manner. The modular layout and the stacking of the printed circuit boards were designed for efficient point to point wiring.

The housing design was accomplished with the techniques of simplicity in design to reduce cost and provide adequate strength to weight ratio to insure meeting the vibration and shock goals.

6.4 MATERIALS

Aluminum type 6061-T6 was selected to be the housing material on the basis of its excellent non-magnetic properties. Although this metal is not the lightest material that could be selected, it is optimum in the trade off between being non-magnetic and lightweight.

6.5 MEMORY ORGANIZATION

Memory organization and circuit design was aimed at minimizing the number of components and power consumption (and hence structure required for heat transfer).

SECTION 7

LOW MAGNETIC FIELD TECHNIQUES AND TESTING

7.1 SCOPE

The work on this project has centered on the study and testing of the magnetic properties of the components to be used in the memory. The study has taken three courses:

7.1.1 LIAISON WITH ASSOCIATED RESEARCH GROUPS

(i.e., associated with magnetic research projects)

Communications were established with the following organizations.

(a) NASA Goddard Space Flight Center
(b) Jet Propulsion Laboratory
(c) Texas Instruments, Inc. Dallas
(d) MIT Instrumentation Laboratory
(e) MIT Lincoln Laboratory

7.1.2 SURVEY OF THE LITERATURE ON THE TOPIC

Use was made of the NASA-STAR document service, the International Aerospace Abstracts and local technical libraries. Many papers on the topic have been accumulated as well as many more read by the Staff. A NASA conference on Non-Magnetic Components was held at JPL shortly after DI/AN was awarded this contract and unfortunately, DI/AN was not aware of the conference until after its completion. DI/AN has contacted some of the principals in the meeting and proceedings and reports were requested.

7.1.3 EXPERIMENTAL SET-UP

A program of component testing was set up by DI/AN. The program used a Hewlett-Packard 429B Flux-Gate Magnetometer Probe. The probe was shielded within a dual concentric cylinder shield of Netic and Conetic alloy.

These alloys, supplied by Perfection Mica Company of Chicago have very high saturation and very low retentivity and thus attenuate stray and ambient fields quite well. The cylinders are 5" in diameter and 12" long.

The Magnetometer Probe is a Vector Instrument, and therefore can be lined up normal to the ambient (mostly earth) magnetic field for a null reading. Since there is a 20,000 gamma ambient horizontal field and the most sensitive scale in 100 gamma, 0.3^{o} of probe rotation will cause a full scale deflection. The simple shield attentuated the earth field by a factor of 12.5 to 1600 gamma. Reduction in long-term interference field variations (due to changes in both magnitude and direction of the field) were less. Before shielding these transients were about 100 gamma and after shielding, about 20 gamma for an improvement of about 5:1. At this shielding level, some measurements could be made on a short term basis where the variation for some periods were less than 5 gamma. The magnetic measurements test facilities were improved so that sensitivities of ±0.5 gamma have been achieved.

In addition to the above work, DI/AN wound a magnetizing (25 gauss) coil which doubles for de-gaussing (400 gauss rms) incoming components.

7.1.4 VENDOR CONTACTS

The following companies were contacted in reference to low magnetic field devices:

(a) Motorola
(b) Fairchild
(c) TRW
(d) Texas Instruments
(e) Kemet

In addition to investigating existing sources of acceptable components, DI/AN investigated new approaches to the magnetic field problem such as:

(a) Ceramic substrate mountings
(b) Epoxy encapsulation
(c) Special lead and bonding techniques

7.2 RESULTS OF INVESTIGATIONS

7.2.1 TAPE-WOUND MAGNETIC CORES

The magnetic fields generated by tape-wound driver cores are not prohibitively large but do produce measurable fields of about one-half the worst-case allowable field.

7.2.2 TRANSISTORS

Tests on transistors showed that the leads are the principle source of magnetic disturbances. Fields were detected even when the leads were cut to the vanishing point. In the case of some diodes, a substantial (greater than 1/16 inch) amount of Kovar lead materials are inside the glass case, thus setting a lower bound on the field. In some cases (Fairchild), nickel is used for the case material, making the situation even worse.

7.3 CONCLUSIONS OF MAGNETIC STUDY

a. Standard transistors and diodes using Kovar leads and/or magnetic cases must not be used, if possible.

b. Large tape-wound driver cores convert magnetic fields which are not prohibitively large but which do produce measurable fields about one-half the worst case allowable field. Since such cores are usually driven by transistors, these cores should not be used in this project if the magnetic specification is to be met or bettered.

7.4 MAGNETIC TESTING

An important design goal of this project is to achieve a low magnetic field external to the memory. In this direction, DI/AN has performed extended in-house testing of both standard and non-standard circuit components. Among those things tested have been resistors, capacitors, diodes, and mechanical parts such as housings, screws, etc. In connection with this program, a standard DI/AN aluminum-magnesium aerospace system housing was sent to the Contract Monitor, Mr. Roger Cliff, for testing at the magnetic facility maintained by NASA at GSFC. Mr. Cliff's report on this mechanical housing was that to within the limits of the measuring capability of the facility, the housing was nonmagnetic. DI/AN thus feels assured that the high quality aluminum and magnesium used are sufficiently pure for use in the aerospace memory project.

7.5 PERMANENT FIELD OF MEMORY CORE PLANES

When dealing with the minute magnetic fields pertinent to this investigation, the collection of 6000 ferrite cores is bound to have significant effect on magnetic state of the system. However, due to their small size, coupled with the closed magnetic path of a toroid, the precise measurement of a core external field is quite difficult. The data presented here are, therefore, very approximate and an error of 2/1 is highly probable.

Tests were first performed on ferrite 50 mil O.D. cores and results were scaled down in a reasonable manner. Worst case measurement on a set of Univac cores showed 1γ at 1". The average disturbance at 1" was about 0.8γ. A set of 64 cores lying flat on a piece of tape was then tested. The cores were arranged in a circular pattern 7/16" in diameter. The unit was tested in various orientations relative to the magnetometer probe. The worst condition of magnetic disturbance (after permanizing) occurred when the plane of the cores was parallel to the measuring axis of the probe and lead to a value of 91γ, or 1.4 per core, somewhat more than the single core measurements indicated. By linear extrapolation at 18" a core plane of 6144 cores will yield a field of:

$$\frac{6144}{5832} \times 1.4 = 1.47\gamma$$

This is a figure obtained for 50 mil O.D. cores and is a substantial portion of the 2γ allowed by the specification. The cores used in the E-1599 memory are 30 mil O.D. cores whose total volume is about 1/5 that of the 50 mil cores and surface area is 1/3 that of the larger cores. In addition, the relative surface areas of the cores affect the close field fringing and the initial rate of decay of the field with distance. As a compromise, the field of a 30 mil core of similar size geometry and material when measured at a point in the R^3 decay region will be about 1/4 that of the 50 mil core. The value of the field at 18" is 0.37, or 1/5 of the total allowable field.

Measurements were done on the 4096 close-packed double core plane built for R-1150. The measuring distance was 1.5". In terms of the core required for E-1599, the field expected is:

$$\frac{4096}{6144} \quad \frac{(1.5)^3}{(18)^3} \quad \frac{(.37)}{3} \quad = 425\gamma$$

and the expected error is ±2/1.

The core plane was tested with the following results. All test distances are 1.5" ±1/4".

Core State	Disturbance
Original	79γ
Approx. 15 Gauss D.C. perm.	100γ
Approx. 500 Gauss de-Gaussing	12γ
Approx. 500 Gauss perming.	560γ

The 500 Gauss perming was obtained by applying an A.C. deGaussing current from a Variac until a circuit breaker suddenly dropped the current to zero. The two perming fields are respectively less than and greater than the 25 Gauss field that caused the worst cases of section 1 and 2 above. The field value measured fell within the predicted range. In percentages, the 425 is closer to the upper worst case of 560 than the lower bound of 100. Since we have always rounded and approximated upwards, this might have been expected.

Conclusion:

A properly designed, closely-packed plane or set of planes of 6144 30 mil O.D. ferrite cores will not give a static magnetic field disturbance of greater than 0.4γ at 18". In the design of the memory, 0.4γ will be allotted to the core planes. The rest of the memory must, therefore, exhibit less than 1.6γ disturbance at 18".

SECTION 8

SELECTION OF DISCRETE COMPONENTS

8.1 SCOPE

In May of 1966, a program was begun to implement the memory system using discrete micro-components. This was done as a back-up in anticipation of the possibility that the hybrid vendors would be unable to meet the stringent requirements placed by DI/AN. The program included an evaluation of various types of transistors, diodes, and resistors to meet the requirements of this memory. The discrete component choices resulting from this study are as follows:

8.2 TRANSISTOR SELECTION

a. Type: Fairchild ceramic FK series.
b. Size: 80 x 80 x 50 mil thick.
c. Lead Length: 0.25 inch minimum.
d. Lead Material: Gold-plated nickel alloy.
e. Package Weight: 0.015 gram.
f. Hermetically sealed.
g. Usage: Military program RAF, Sylvania, Raytheon and NASA.
h. May be purchased to Fairchild Fact Program.

8.2.1 The Fairchild FK transistor was recommended for this project for the following reasons:

a. Small size.
b. Low cost.
c. Quick delivery time.
d. Ease of use in module packaging
e. Previous NASA usage with success.

Even though the lead material is magnetic, the FK transistor lead mass is small enough to produce a magnetic field that will be well within NASA specifications.

8.3 DIODE SELECTION

a. Type: Microsemiconductor Corp., MC-9889 (electrically equivalent to 1N914) micro-diode.
b. Size: .065 x 0.1 inch maximum.
c. Lead Length: 1.0 inch minimum.
d. Lead Material: Alloy 180 (non-magnetic).
e. Reliability: MIL-S-19500B.

8.4 RESISTOR SELECTION

a. Type: Bourns, Inc., Cermet Resistor Element Model 4200.
b. Lead Material: Alloy 180 (non-magnetic).
c. Size: 0.1 x 0.03 x .055 inches maximum.
d. Usage: Poseidon Program, Naval Ordnance Labs., Hughes Aircraft.
e. Meets: MIL-R-10509E.
f. Power Rating: 70 milliwatts.

8.5 CAPACITOR SELECTION TYPES

a. Vitramon, VY series - solid state porcelain capacitor (glass dielectric).
    a. Lead Material: Solder coated silver (non-magnetic).
b. Electron Products, EPC series - ceramic capacitor.
    a. Lead Material: Tin coated copper (non-magnetic).
c. Kemet, KG series - polar, solid tantalum capacitor.
    a. Lead Material: Alloy 180 (non-magnetic).
    b. Case material - Brass.
    c. Hermetic seal.

8.6 SENSE AMPLIFIER SELECTION

a. Motorola Type SC1219F (formerly XC-87).
b. Ceramic flat-pack.
c. Kovar Leads
    a. Leads are magnetic but will be cut short to reduce the magnetic disturbance.

8.7 CONNECTOR SELECTION

a. Cannon; non-magnetic connector type DDM-50-P-NMC.

   a. Magnetic flux density less than 20 gamma after magnetization with a 5000 gauss magnet.

SECTION 9

PACKAGING TECHNIQUES

9.1 CIRCUIT BOARD DESCRIPTION

The memory contains six printed circuit boards of dimensions 3.5 x 4.0 x 1/16 inches. The etch is solder-plated copper. Below is a table listing the types and quantity of boards required.

a. Driver Board (1 required): This board contains 20 core driver modules, two current sources and seven address input circuits.

b. A-Bit Board (2 required): This board contains five bits each consisting of a sense amplifier, Z-Driver, Data-Output One-Shot, and Data Input circuit.

c. B-Bit Board (1 required): This board contains two bits as described above plus two core drivers and two Address Input circuits.

d. Control Chain Board: This board contains the one-shots required to generate the control timing for the memory system.

e. Memory Plane: This board contains twelve 32 x 16 folded core planes and twelve diode packs, each consisting of 4 diode pairs.

9.2 MODULE CONFIGURATION AND SIZE

A study was made to determine the smallest DI/AN module size to package each circuit using the microcomponents selected in Section 8.0. The size of the Pico-Bit is 3/8 x 5/8 x .350 and the size of the Miniature Square is 9/16 x 25/32 x .350. Below is a table listing the packaging of the modules in the system.

Circuit	Package Size
Universal One-Shot (UOS-1)	Pico-Bit
Line Driver (DPN-7)	Pico-Bit
Data Interface Network (DIN-3)	Pico-Bit
Address Interface Network (DIN-4)	Pico-Bit
Z Driver (ZD-2)	Pico-Bit
Current Source	Pico-Bit
Mode Interface	Min. Square
Auxiliary Amplifier #1	Pico-Bit
Auxiliary Amplifier #2	Pico-Bit
Data Amplifier	Pico-Bit
Sense Power Enable-Strobe	Min. Square
Mode Amplifier	Pico-Bit

All modules are tested electrically over the temperature range and tested magnetically before acceptance.

9.3 SYSTEM CARD ASSEMBLY AND HARNESS WIRING

The techniques of twisting power lines around the proper ground return and of avoiding all wiring or etch loops have been utilized to reduce the dynamic magnetic field and to reduce possibility of excessive noise pick-up.

In addition, to reduce interwiring noise, the power lines have been located as far as possible from sensitive signal regions. The ground wires for the Z-Drivers, Line Drivers, Sense Amplifiers and One-Shots are separated in the interboard wiring and meet at the common ground point close to the connector.

9.4 HOUSING

The housing has been designed for minimum volume to meet the required environmental conditions. All housing materials are non-magnetic. The housing material is Aluminum (6061-T6), the screws are stainless steel 316 and the heli-coils are stainless steel 303.

SECTION 10

RELIABILITY TECHNIQUES

10.1 DESIGN PHILOSOPHY

DI/AN employed various techniques, both in the design and fabrication stages, to assure a memory of high reliability. In the design phase, emphasis was placed on logical organization and circuit design to minimize the number of components used. Circuit redundancy was used in certain critical areas and safety margins or derating was provided for all components. Integrated circuits were used where possible, for their potential future reliability.

10.2 QUALITY CONTROL

During manufacture, emphasis on reliability continued. Quality Control and Inspection Departments are intimately involved during the life of a program. Surveillance by the departments applies from receipt of components through production to final equipment inspection and acceptance. An active program for the training and certification of solderers to NASA standards is conducted under the full time supervision of a NASA-certified instructor, which provides DI/AN with a pool of competent NASA-certified manufacturing personnel. This personnel was used on the memory construction phase.

10.3 INTERCONNECTION REDUCTION IN CORE STACK

DI/AN Controls has advanced the technique that makes it more practical to produce a core stack where the X wires and the Y wires are continuous throughout the stack, thus eliminating the usual two connections for every X and Y wire in every core plane. Many of the usual restrictions on such a stack construction method are eliminated. For example, one method restricts such stack to no more than ten planes per assembly, because of the difficults in testing and repairs. The stacks produced by this technique also have long slack loops in the access lines on the edges of the stack perpendicular to the fold lines. These long slack lines increase the drive line resistance and inductance, and also offer additional opportunity for wire breakage. Another technique in common use makes a similar type of stack, but pulls the stack loops tight. This removes the additional wire, but increases the chance of wire damage because of the large amount of wire pulled through the planes to tighten the slack loops.

DI/AN Controls designed and built an evaluation model of a stack of unique core and winding layout and an unconventional winding method. This method of core stack construction was utilized in the memory described in this document and offers the following advantages:

1. The X and Y wires run continuously through the stack, with no joints between bit-planes.
2. No slack loops are formed during stack construction, therefore, no slack loops are left in the finished stack. In addition, there are no slack loops to be pulled tight after the stack is constructed.
3. A smaller physical size and lower stack impedance than with conventional methods of core and winding layout is achieved.

See Figure 10-1 for a photograph of a 4096-bit core plane constructed using this technique. Packing density is 63,000 bits per cubic inch.

10.4 RELIABILITY ESTIMATE

The majority of the electrical components used in this memory are unique, both in terms of size and in the use of low-magnetic material in the component leads and other areas. Therefore, valid reliability data on the components used does not exist. Because of this, no formal quantitative reliability prediction was performed on this system.

A complete component parts list is provided in Appendix B.

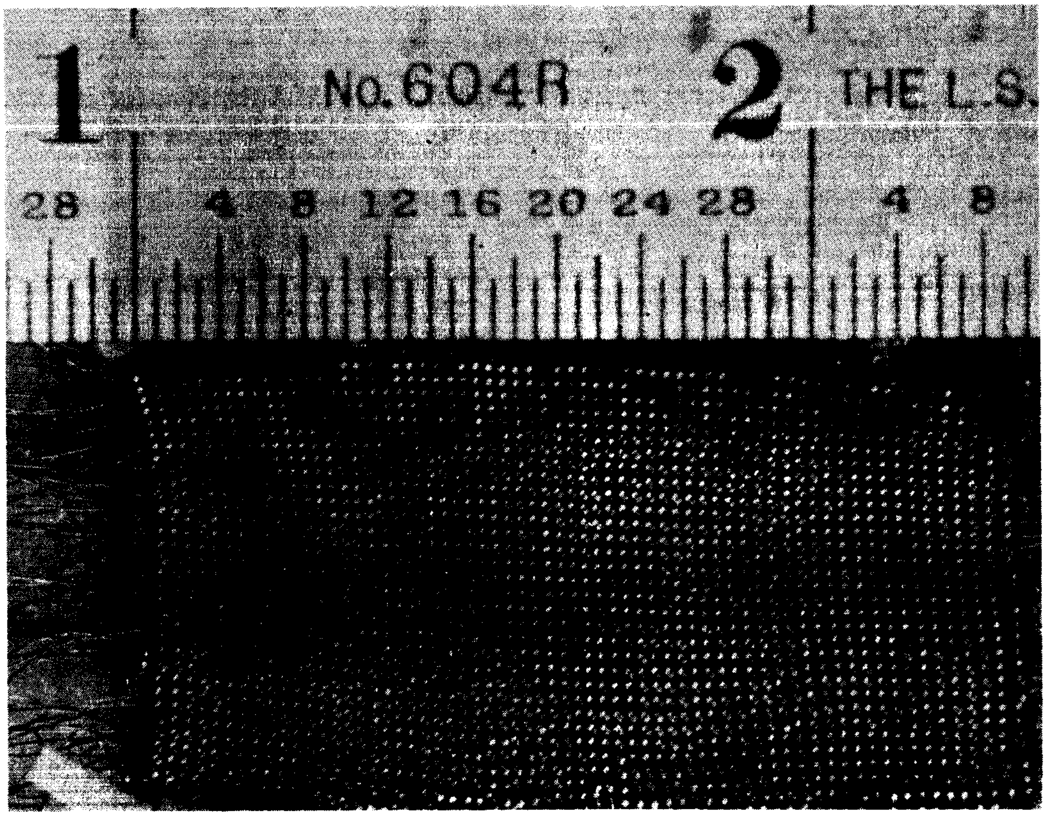


Figure 10-1. Developmental 4096-Bit Core Plane, 0.030" O.D. Cores.

SECTION 11

PROJECT RESULTS AND CONCLUSIONS

The goal of this project was to develop and produce a Random Access Memory of 512 words of 12 bits per word. This memory is to be used in a prototype spaceborne general purpose data processor.

The criteria of this memory, i.e., reliability, low power drain, light weight, small size, and low magnetic signature have been achieved. The techniques of power enabling and complementary transistor circuit design were utilized to achieve low power drain.

A literature search, combined with extensive research and testing at DI/AN Controls in the field of low magnetic techniques have resulted in the development of a memory system which is essentially non-magnetic. Careful attention was given to circuit design which utilizes a minimum count of components and the components were of the microminiature type which greatly reduced the size and weight of this memory. Integrated circuits were also used to increase the reliability as well as to reduce both size and weight. These reductions were estimated to be 50% compared to existing memories of this storage capacity.

The research, development and production of this memory system is a significant advancement in the state of the art. The techniques developed in this program and the knowledge gained can have many applications in the field of aerospace research where the requirements of size, weight, power consumption and low magnetic disturbances are of a critical nature.

APPENDIX B

COMPONENT PARTS LIST
LOW POWER MEMORY
NAS 5-9064
PROJECT E-1599

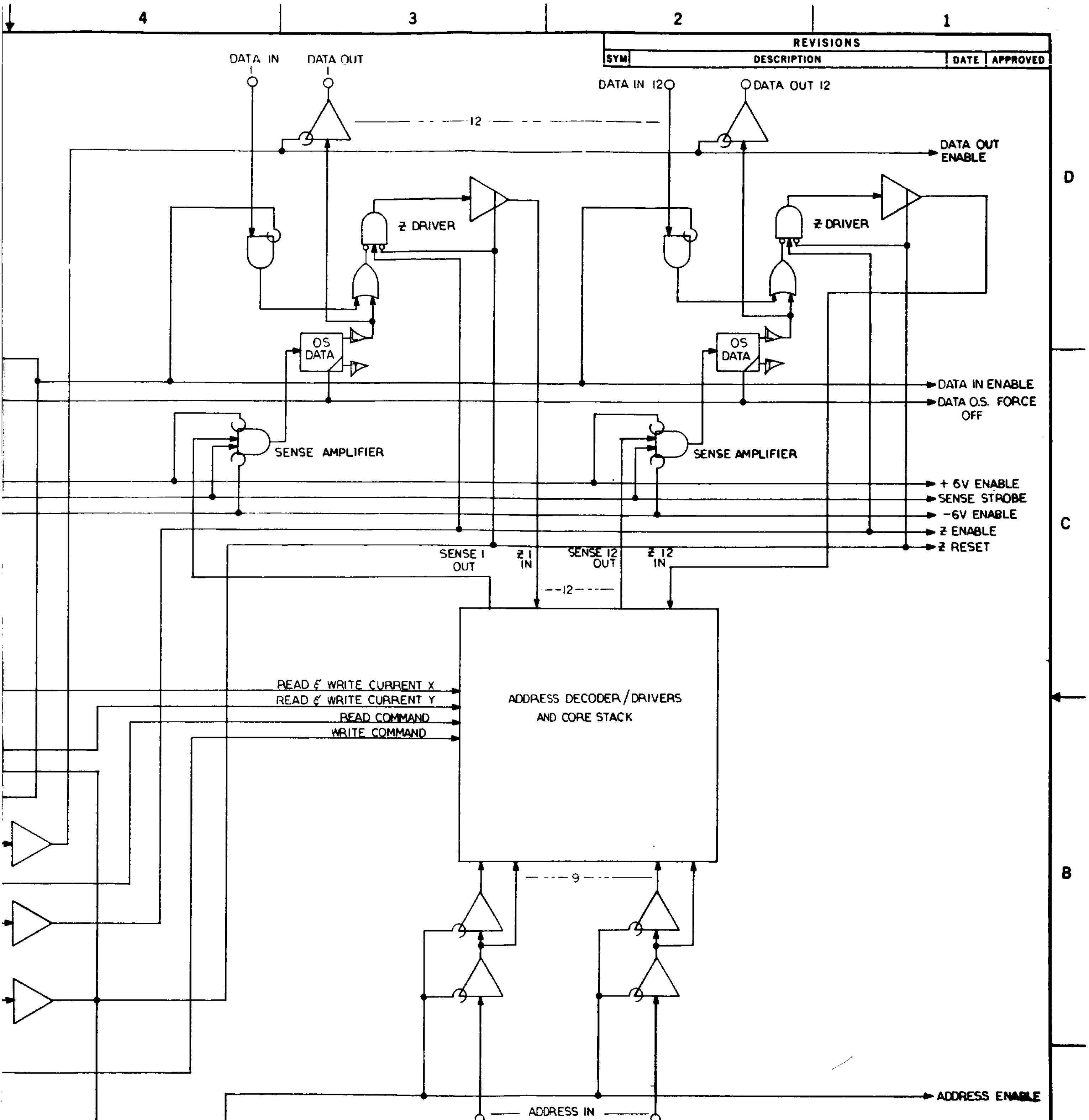
ITEM	QTY.	PART NO.	DESCRIPTION
1	23	7040-119-001	Transistor, FK3502, Fairchild
2	181	7040-118-001	Transistor, FK3300, Fairchild
3	53	7040-116-001	Transistor, FK2894, Fairchild
4	84	7040-115-001	Transistor, FK914, Fairchild
5	25	7040-117-001	Transistor, FK3251, Fairchild
6	359	7050-076-015	Diode, MC-9889 Micro Semi-Conductor Corp.
7	39	7010-6030-02	Resistor, 9100 Ohms, ±2% 4200A-105-9101G, Bourns
8	55	7010-6029-02	Resistor, 6800 Ohms, ±2% 4200A-105-6801G, Bourns
9	14	7010-6028-02	Resistor, 6200 Ohms, ±2% 4200A-105-6201G, Bourns
10	12	7010-6027-02	Resistor, 5600 Ohms, ±2% 4200A-105-5601G, Bourns
11	43	7010-6026-02	Resistor, 5100 Ohms, ±2% 4200A-105-5101G, Bourns
12	12	7010-6025-02	Resistor, 4700 Ohms, ±2% 4200A-105-4701G, Bourns
13	24	7010-6024-02	Resistor, 4300 Ohms, ±2% 4200A-105-4301G, Bourns
14	1	7010-6023-02	Resistor, 3900 Ohms, ±2% 4200A-105-3901G, Bourns
15	42	7010-6022-02	Resistor, 3600 Ohms, ±2% 4200A-105-3601G, Bourns
16	37	7010-6021-02	Resistor, 2700 Ohms, ±2% 4200A-105-2701G, Bourns
17	20	7010-6020-02	Resistor, 2400 Ohms, ±2% 4200A-105-2410G, Bourns
18	26	7010-6019-02	Resistor, 2200 Ohms, ±2% 4200A-105-2201G, Bourns
19	15	7010-6018-02	Resistor, 1800 Ohms, ±2% 4200A-105-1801G, Bourns
20	52	7010-6016-02	Resistor, 1200 Ohms, ±2% 4200A-105-1201G, Bourns
21	1	7010-6015-02	Resistor, 1000 Ohms, ±2% 4200A-105-1001G, Bourns
22	12	7010-6014-02	Resistor, 910 Ohms, ±2% 4200A-105-9100G, Bourns
23	15	7010-6013-02	Resistor, 820 Ohms, ±2% 4200A-105-8200G, Bourns
24	26	7010-6012-02	Resistor, 680 Ohms, ±2% 4200A-105-6800G, Bourns
25	1	7010-6011-02	Resistor, 560 Ohms, ±2% 4200A-105-5600G, Bourns

APPENDIX B (continued)

ITEM	QTY.	PART NO.	DESCRIPTION
26	2	7010-6010-02	Resistor, 430 Ohms, ±2% 4200A-105-4300G, Bourns
27	1	7010-6009-02	Resistor, 390 Ohms, ±2% 4200A-105-3900G, Bourns
28	52	7010-6008-02	Resistor, 330 Ohms, ±2% 4200A-105-3300G, Bourns
29	1	7010-6007-02	Resistor, 270 Ohms, ±2% 4200A-105-2700G, Bourns
30	12	7010-6006-02	Resistor, 240 Ohms, ±2% 4200A-105-2400G, Bourns
31	1	7010-6005-02	Resistor, 220 Ohms, ±2% 4200A-105-2200G, Bourns
32	6	7010-6004-02	Resistor, 180 Ohms, ±2% 4200A-105-1800G, Bourns
33	12	7010-6003-02	Resistor, 120 Ohms, ±2% 4200A-105-1200G, Bourns
34	1	7010-6002-02	Resistor, 91 Ohms, ±2% 4200A-105-91ROG, Bourns
35	32	7010-6001-02	Resistor, 51 Ohms, ±2% 4200A-105-51ROG, Bourns
36	23	7010-6038-02	Resistor, 100K, ±2% 4200A-105-1003G, Bourns
37	21	7010-6037-02	Resistor, 62K, ±2% 4200A-105-6202G, Bourns
38	2	7010-6036-02	Resistor, 47K, ±2% 4200A-105-4702G, Bourns
39	23	7010-6035-02	Resistor, 33K, ±2% 4200A-105-3302G, Bourns
40	2	7010-6034-02	Resistor, 18K, ±2% 4200A-105-1802G, Bourns
41	2	7010-6033-02	Resistor, 15K, ±2% 4200A-105-1502G, Bourns
42	21	7010-6032-02	Resistor, 13K, ±2% 4200A-105-1302G, Bourns
43	9	7010-6031-02	Resistor, 12K, ±2% 4200A-105-1202G, Bourns
44	2	7010-1693-14	Fixed Film Resistor, 22 Ohms 1/2 watt type RL20
45	12		Wire Wound Res. RCL Type 7007 9.2 ±1% Ohms +400 ±40 ppm/°C
46	2	7010-1244-12	Fixed Film Resistor, 91 Ohms 1/4 watt type RL07
47	24	7010-0568-14	Fixed Comp. Res., 150 Ohms ±5%, 1/8 w, type RC05
48	4	7010-0600-14	Fixed Comp. Res., 3300 Ohms, ±5%, 1/8 w, type RC05
49	2	7010-0602-14	Fixed Comp. Res., 3900 Ohms, ±5%, 1/8 w, type RC05
50	2	7010-0630-14	Fixed Comp. Res., 56K Ohms, ±5%, 1/8 w, type RC05
51	13	7010-0636-14	Fixed Comp. Res., 100K Ohms, ±5%, 1/8 w, type RC05
52	3		Marshall Industries Type EPC 20x100-M 10pf Capacitor
53	1		Marshall Industries Type EPC 20x220-M 22pf Capacitor
54	12		Marshall Industries Type EPC 20x330-K 33pf Capacitor

APPENDIX B (continued)

ITEM	QTY.	PART NO.	DESCRIPTION
55	2		Marshall Industries Type EPC 20x471-M 470pf Capacitor
56	14		Marshall Industries Type EPC 20x102-M 1000pf Capacitor
57	12		Marshall Industries Type EPC 20x332-K 3300pf Capacitor
58	2		Vitramon Type VY13C101J 100pf Capacitor
59	3		Vitramon Type VY13C151J 150pf Capacitor
60	14	7020-0295-05	Kemet Type K615J20KMS 15uf Capacitor
61	1	7020-0296-05	Kemet Type KG10J20KMS 10uf Capacitor
62	1	712-0012-800	Cannon Rectangular Connector



REVISIONS			
SYM	DESCRIPTION	DATE	APPROVED

QTY.	NOMENCLATURE OR DESCRIPTION	CODE IDENT.	PART NO.	SPEC.	ITEM NO.

LIST OF MATERIALS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON:
ANGLES, ± 0°30'
FRACTIONS, ± 1/64
DECIMALS, .XX ± .030
.XXX ± .005

MATERIAL: —

FINISH: —

NEXT ASSY.	USED ON
APPLICATION	

DRAWN R. Maguood 3 NOV 66
CHECKED M. Meson 3 Nov. 66
PROJECT ENGINEER A. C. Allen 4 Nov. 66
PRODUCT ENGINEER
REFERENCE
PROJECT APPROVAL
PROJECT E1599

A

Di/An Controls, Inc.
BOSTON, MASS.

LOGIC SCHEMATIC
LOW POWER MEMORY SYSTEM

CODE IDENT.	SIZE		
06900	D	2204-4009	—

SCALE — SHEET 1 OF 1

4 3 2 1